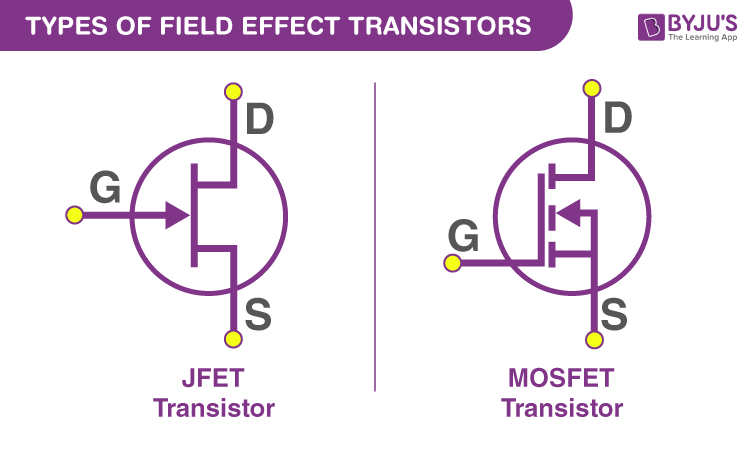
***FET***

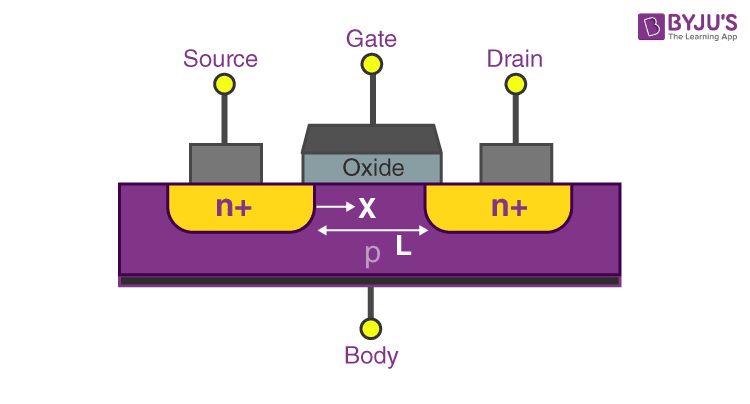
### ****Types of FETs:****

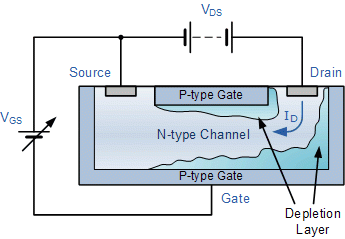
There are two types of Field Effect Transistors:

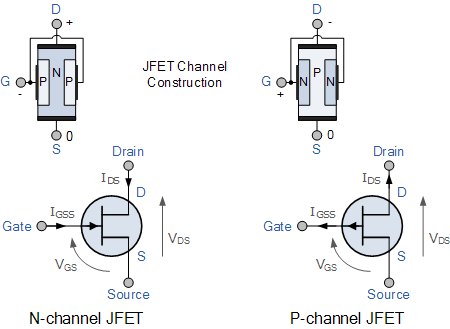
* Junction Field Effect Transistor (JFET)
* Metal oxide semiconductor Field Effect Transistor (MOSFET)



### ****Essential Information concerning FETs****









### Comparison of Connections between a JFET and a BJT

|  |  |
| --- | --- |
| Bipolar Transistor (BJT) | Field Effect Transistor (FET) |
| Emitter – (E)     >>     Source – (S) | |
| Base – (B)     >>     Gate – (G) | |
| Collector – (C)     >>     Drain – (D) | |

There are two types of FET’s one will be in which the current is taken primarily by majority carriers and thus are **majority charge carrier devices**. The other will be where the current flow is primarily due to the minority carriers and thus are called **minority charge carrier devices**. The electrons flow to the drain from the source through active channels in the device. The ohmic contacts connect both the terminal conductors to the [semiconductors](https://byjus.com/jee/semiconductors/). The source terminal and the gate have a potential between them and the conductivity of the channel is a function of it.

There are three terminals when it comes to FET:

* ISis the term used for the current that enters through our first terminal that is the source.
* ID is the term used for the current that leaves the channel through the drain (D). The voltage between drain to source is VDS .
* The channels conductivity is modulated by the gate (G). ID can be controlled by applying a voltage at G.

The functions of the above-mentioned gates explain their names. The working of these gates is similar to a gate in real life as in the terminal controls when they open and when they close. The gate can either choose to permit the passage of electrons or stop it.

**What is a Junction Field Effect Transistor?**

A JFET is a semiconductor with 3 terminals, available either in N-channel or P-channel types. It is unipolar but has similar characteristics as of its Bipolar cousins. Instead of PN junctions, a JFET uses an N-type or P-type semiconductor material between the collector and emitter (Source & Drain). The N-type material is made by doping Silicon with donor impurities so that the current flowing through it is negative. Similarly, the P-type material is doped with acceptor impurities so the current flowing through them is positive. N-type JFET is more commonly used because they are more efficient due to the fact that electrons have high mobility.

**CHARACTERISTICS OF JFETS**

There are two types of static characteristics viz

(1) Output or drain characteristic and

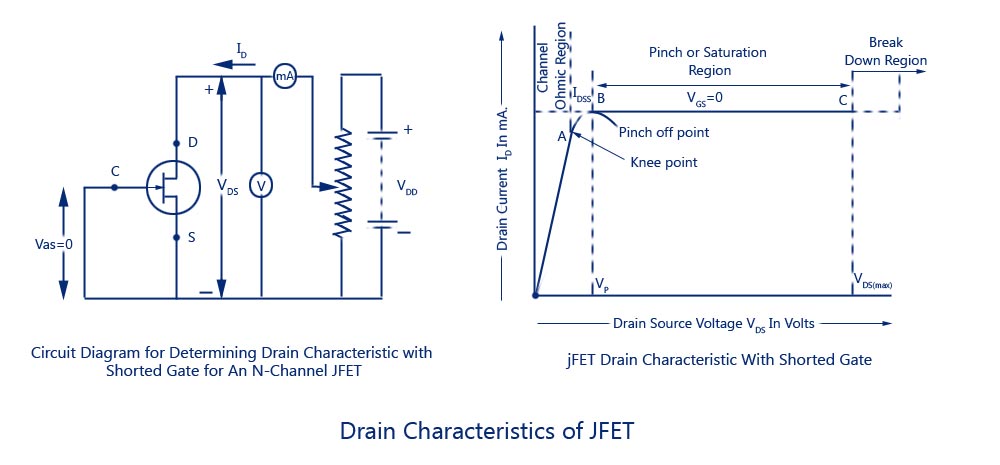
(2) Transfer characteristic.

**1. *Output or Drain Characteristic.***

The curve drawn between drain current Ip and drain-source voltage VDS with gate-to source voltage VGS as the parameter is called the *drain*or *output characteristic.*This characteristic is analogous to collector characteristic of a BJT:

**(a) Drain Characteristic with Shorted-Gate**

The circuit diagram for determining the drain characteristic with shorted-gate for an N-channel JFET is given in figure. and the drain characteristic with shorted-gate is shown in another figure.

[](https://www.circuitstoday.com/wp-content/uploads/2009/08/Drain-Characteristics-of-JFET.jpg)

**Drain-Characteristics-of-JFET**

Initially when drain-source voltage Vns is zero, there is no attracting potential at the drain, so no current flows inspite of the fact that the channel is fully open. This gives drain current Ip = 0. For small applied voltage Vna, the N-type bar acts as a simple semiconductor resistor, and the drain current increases linearly with\_the increase in Vds, up to the knee point. This region, (to the left of the knee point) of the curve is called the channel ohmic*region,*because in this region the FET behaves like an ordinary resistor.

With the increase in drain current ID, the ohmic voltage drop between the source and channel region reverse-biases the gate junction. The reverse-biasing of the gate junction is not uniform throughout., The reverse bias is more at the drain end than that at the source end of the channel, so with the increase in Vds, the conducting portion of the channel begins to constrict more at the drain end. Eventually, a voltage Vds is reached at which the channel is pinched off. The drain current ID no longer increases with the increase in Vds. It approaches a constant saturation value. The value of voltage VDS at which the channel is pinched off (i.e. all the free charges from the channel get removed), is called the *pinch-off voltage*Vp. The pinch-off voltage Vp, not too sharply defined on the curve, where the drain current ID begins to level off and attains a constant value. From point A (knee point) to the point B (pinch-off point) the drain current ID increases with the increase In voltage Vds following a reverse square law. The region of the characteristic in which drain current ID remains fairly constant is called *the pinch-off region.*It is also sometimes called the *saturation region*or *amplifier region.*In this region the JFET operates as a *constant current device since*drain current (or output current) remains almost constant. It is the normal operating region of the JFET when used as an amplifier. The drain current in the pinch-off region with VGS = 0 is referred to the *drain-source saturation current, Idss*).

It is to be noted that in the pinch-off (or saturation) region the channel resistance increases in proportion to increase in VDS and so keeps the drain current almost constant and the reverse bias required by the gate-channel junction is supplied entirely by the voltage drop across the channel resistance due to flow of IDsg and not by the external bias because VGS = 0

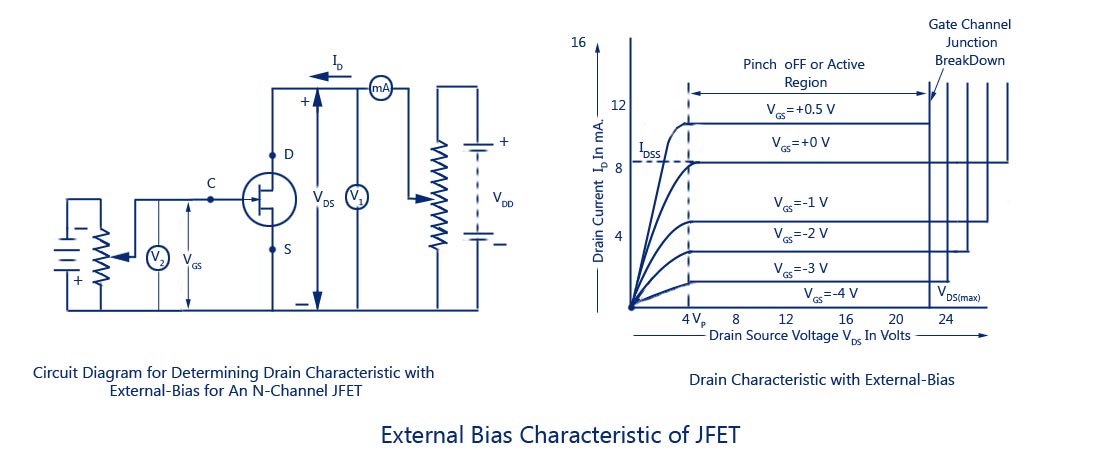
Drain current in the pinch-of region is given by Shockley’s equation

where ID is the drain current at a given gate-source voltage VGS, IDSS is the drain-current with gate shorted to source and VGS (0FF) is the gate-source cut-off voltage.

If the drain-source voltage, Vds is continuously increased, a stage comes when the gate-channel junction breaks down. At this point current increases very rapidly. and the JFET may be destroyed. This happens because the charge carriers making up the saturation current at the gate channel junction accelerate to a high velocity and produce an *avalanche effect.*

***Drain Characteristics with External Bias***

The circuit diagram for determining the drain characteristics with different values of external bias is shown in figure. and a family of drain characteristics for different values of gate-source voltage VGS is given in next figure

[](https://www.circuitstoday.com/wp-content/uploads/2009/08/External-Bias-Characteristic-of-JFET.jpg)

It is observed that as the negative gate bias voltage is increased

(1) The maximum saturation drain current becomes smaller because the conducting channel now becomes narrower.

(2) Pinch-off voltage is reached at a lower value of drain current ID than when VGS = 0. When an external bias of, say – 1 V is applied between the gate and the source, the gate-channel junctions are reverse-biased even when drain current, ID is zero. Hence the depletion regions are already penetrating the channel to a certain extent when drain-| source voltage, VDS is zero. Due to this reason, a smaller voltage drop along the channel (i.e. smaller than that for VGS = 0) will increase the depletion regions to the point where 1 they pinch-off the current. Consequently, the pinch-off voltage VP is reached at a lower 1 drain current, ID when VGS = 0.

(3) The ohmic region portion decreases.

(4) Value of drain-source voltage VDS for the avalanche breakdown of the gate junction is reduced.

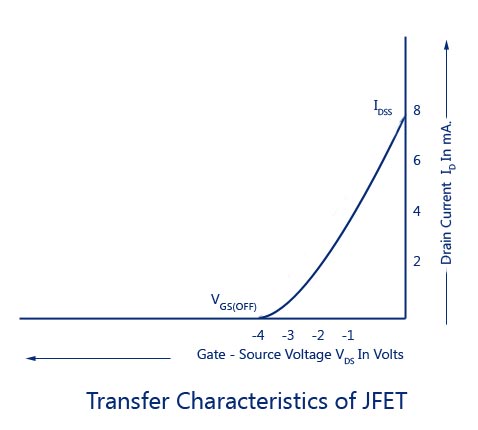
Value of drain-source voltage, VDS for breakdown with the increase in negative bias voltage is reduced simply due to the fact that gate-source voltage, VGS keeps adding to the I reverse bias at the junction produced by current flow. Thus the maximum value of VDS I that can be applied to a FET is the lowest voltage which causes avalanche breakdown. It is also observed that with VGS = 0, ID saturates at IDSS and the characteristic shows VP = 4 V. When an external bias of – 1 V is applied, the gate-channel junctions still require -4 V to achieve pinch-off. It means that a 3 V drop is now required along the channel instead of the previous 4.0 V. Obviously, this drop of 3 V can be achieved with a lower value of drain current, Similarly when VGS = – 2 V and – 3 V, pinch-off is achieved with 2 V and 1 V respectively, along the channel. These drops of 2 V and 1 V are, of course, achieved with further reduced values of drain current, ID. It is further observed that when the gate-source bias is numerically equal to pinch-off voltage, VP (-4 V in this case), no channel drop is required and, therefore, drain current, ID is zero. The gate-source bias voltage required to reduce drain current, ID to zero is designated the gate-source cut-off voltage, VGS /0FF) and, as explained,

Hence for working of JFET in the pinch-off or active region it is necessary that the following conditions be fulfilled.

VP< VDS< VDS (max)

VGS (OFF)< VGS< 0

0 < ID < IDSS

[](https://www.circuitstoday.com/wp-content/uploads/2009/08/Transfer-Characteristics-of-JFET.jpg)

**2. *Transfer Characteristic of JFET***

The transfer characteristic for a JFET can be determined experimentally, keeping drain-source voltage, *VDS*constant and determining drain current, ID for various values of gate-source voltage, VGS. The circuit diagram is shown in fig. 9.7 (a). The curve is plotted between gate-source voltage, VGS and drain current, ID, as illustrated in fig. *9.8.*It is similar to the transconductance characteristic of a vacuum tube or a transistor. It is observed that

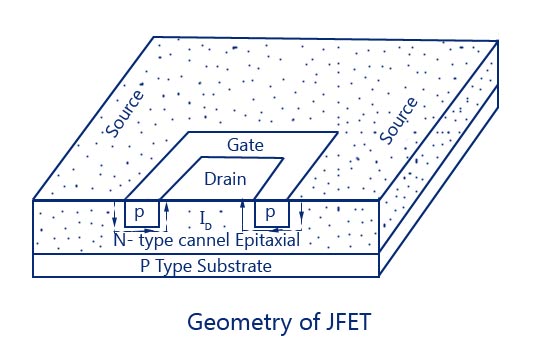
*(i)*Drain current decreases with the increase in negative gate-source bias

*(ii)*Drain current, ID = IDSS when VGS = 0

*(iii)*Drain current, ID = 0 when VGS = VDThe transfer characteristic follows equation (9.1)

The transfer characteristic can also be derived from the drain characteristic by noting values of drain current, IDcorresponding to various values of gate-source voltage, VGS for a constant drain-source voltage and plotting them.

It may be noted that a P-channel JFET operates in the same way and have the similar characteristics as an N-channel JFET except that channel carriers are holes instead of electrons and the polarities of VGS and VDS are reversed.

[](https://www.circuitstoday.com/wp-content/uploads/2009/08/Geometry-of-JFET.jpg)

**MERITS AND DEMERITS OF JFETS**

Junction field effect transistors combine several merits of both conventional (or bipolar) transistors and vacuum tubes. Some of these are enumerated below:

1. Its operation depends upon the flow of majority carriers only, it is, therefore, a unipolar (one type of carrier) device. On the other hand, in an ordinary transistor, both majority and minority carriers take part in conduction and, therefore, an ordinary transistor is sometimes called the bipolar transistor. The vacuum tube is another example of a unipolar device.’

2. It is simpler to fabricate, smaller in size, rugged in construction and has longer life and higher efficiency. Simpler to fabricate in IC form and space requirement is also lesser.

3. It has a high input impedance (of the order of 100 M Q), because its input circuit (gate to source) is reverse biased, and so permits high degree of isolation between the input and the output circuits. However, the input circuit of an ordinary transistor is forward biased and, therefore, an ordinary transistor has low input impedance.

4. It carries very small current because of the reverse biased gate and, therefore, it operates just like a vacuum tube where control grid (corresponding to the gate in JFET) carries extremely small current and input voltage controls the output current. This is the reason that JFET is essentially a voltage driven device (ordinary transistor is a current operated device since input current controls the output current.)

5.    An ordinary transistor uses a current into its base for controlling a large current between collector and emitter whereas in a JFET voltage on the gate (base) terminal is used for controlling the drain current (current between drain and source). Thus an ordinary transistor gain is characterized by current gain whereas the JFET gain is characterized as the trans conductance (the ratio of drain current and gate-source voltage).

6.    JFET has no junction like an ordinary transistor and the conduction is through bulk material current carriers (N-type or P-type semiconductor material) that do not cross junctions. Hence the inherent noise of tubes (owing to high-temperature operation) and that of ordinary transistors (owing to junction transitions) is not present in JFET.

7.    It is relatively immune to radiation.

8.    It has negative temperature coefficient of resistance and, therefore, has better thermal stability.

9.    It has high power gain and, therefore, the necessity of employing driver stages is eliminated.

10.    It exhibits no offset voltage at zero drain current and, therefore, makes an excellent signal chopper.

11.    It has square law characteristics and, therefore, it is very useful in the tuners of radio and TV receivers.

12.    It has got a high-frequency response.

**The main drawback of JFET are:**

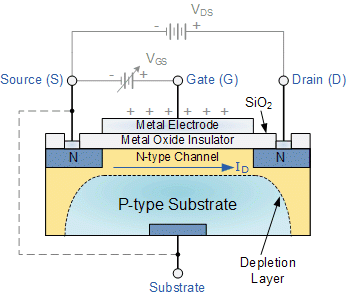
1. Its relative small gain-bandwidth product in comparison with that of a conventional transistor.

2. Greater susceptibility to damage in its handling.

3. JFET has low voltage gains because of small transconductance.

4. Costlier when compared to BJT’s

***MOSFET***



The most common type of insulated gate FET which is used in many different types of electronic circuits is called the **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

The **IGFET** or **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.

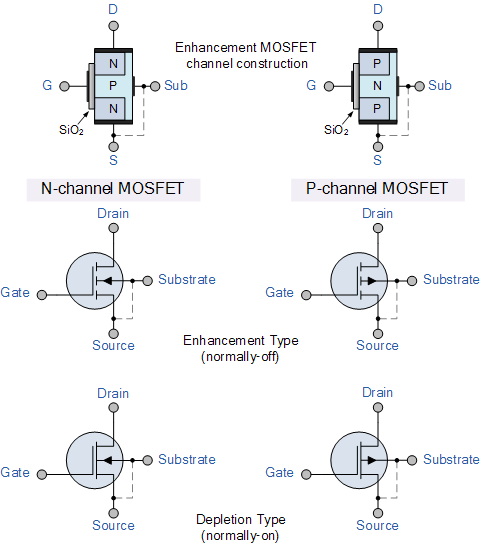
This ultra thin insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the **MOSFET** extremely high way up in the Mega-ohms ( MΩ ) region thereby making it almost infinite.

As the Gate terminal is electrically isolated from the main current carrying channel between the drain and source, “NO current flows into the gate” and just like the JFET, the MOSFET also acts like a voltage controlled resistor where the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also like the JFET, the MOSFETs very high input resistance can easily accumulate large amounts of static charge resulting in the **MOSFET** becoming easily damaged unless carefully handled or protected.

Like the previous JFET tutorial, MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

* Depletion Type   –   the transistor requires the Gate-Source voltage, ( VGS ) to switch the device “OFF”. The depletion mode MOSFET is equivalent to a “Normally Closed” switch.
* Enhancement Type   –   the transistor requires a Gate-Source voltage, ( VGS ) to switch the device “ON”. The enhancement mode MOSFET is equivalent to a “Normally Open” switch.

The symbols and basic construction for both configurations of MOSFETs are shown below.



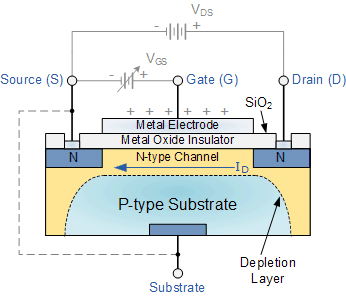
The four MOSFET symbols above show an additional terminal called the Substrate and is not normally used as either an input or an output connection but instead it is used for grounding the substrate. It connects to the main semiconductive channel through a diode junction to the body or metal tab of the MOSFET.

Usually in discrete type MOSFETs, this substrate lead is connected internally to the source terminal. When this is the case, as in enhancement types it is omitted from the symbol for clarification.

The line in the MOSFET symbol between the drain (D) and source (S) connections represents the transistors semiconductive channel. If this channel line is a solid unbroken line then it represents a “Depletion” (normally-ON) type MOSFET as drain current can flow with zero gate biasing potential.

If the channel line is shown as a dotted or broken line, then it represents an “Enhancement” (normally-OFF) type MOSFET as zero drain current flows with zero gate potential. The direction of the arrow pointing to this channel line indicates whether the conductive channel is a P-type or an N-type semiconductor device.

**Basic MOSFET Structure and Symbol**



The construction of the Metal Oxide Semiconductor FET is very different to that of the Junction FET. Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers, electrons for n-channel or holes for P-channel, through the semiconductive drain-source channel. The gate electrode is placed on top of a very thin insulating layer and there are a pair of small n-type regions just under the drain and source electrodes.

We saw in the previous tutorial, that the gate of a junction field effect transistor, JFET must be biased in such a way as to reverse-bias the pn-junction. With a insulated gate MOSFET device no such limitations apply so it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve).

This makes the MOSFET device especially valuable as electronic switches or to make logic gates because with no bias they are normally non-conducting and this high gate input resistance means that very little or no control current is needed as MOSFETs are voltage controlled devices. Both the p-channel and the n-channel MOSFETs are available in two basic forms, the **Enhancement** type and the **Depletion** type.

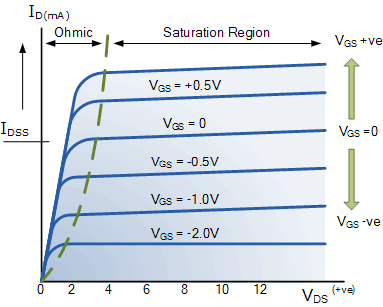
**Depletion-mode MOSFET**

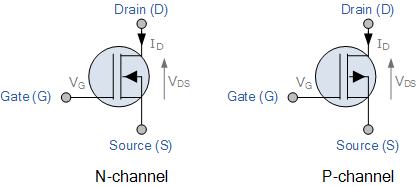
The **Depletion-mode MOSFET**, which is less common than the enhancement mode types is normally switched “ON” (conducting) without the application of a gate bias voltage. That is the channel conducts when VGS = 0 making it a “normally-closed” device. The circuit symbol shown above for a depletion MOS transistor uses a solid channel line to signify a normally closed conductive channel.

For the n-channel depletion MOS transistor, a negative gate-source voltage, -VGS will deplete (hence its name) the conductive channel of its free electrons switching the transistor “OFF”. Likewise for a p-channel depletion MOS transistor a positive gate-source voltage, +VGS will deplete the channel of its free holes turning it “OFF”.

In other words, for an n-channel depletion mode MOSFET: +VGS means more electrons and more current. While a -VGS means less electrons and less current. The opposite is also true for the p-channel types. Then the depletion mode MOSFET is equivalent to a “normally-closed” switch.

**Depletion-mode N-Channel MOSFET and circuit Symbols**





The depletion-mode MOSFET is constructed in a similar way to their JFET transistor counterparts were the drain-source channel is inherently conductive with the electrons and holes already present within the n-type or p-type channel. This doping of the channel produces a conducting path of low resistance between the Drain and Source with zero Gate bias.

**Enhancement-mode MOSFET**

The more common **Enhancement-mode MOSFET** or eMOSFET, is the reverse of the depletion-mode type. Here the conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally “OFF” (non-conducting) when the gate bias voltage, VGS is equal to zero. The circuit symbol shown above for an enhancement MOS transistor uses a broken channel line to signify a normally open non-conducting channel.

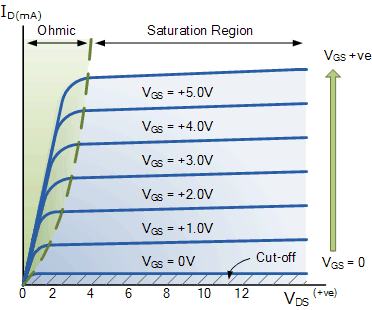
For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage ( VGS ) is applied to the gate terminal greater than the threshold voltage ( VTH ) level in which conductance takes place making it a transconductance device.

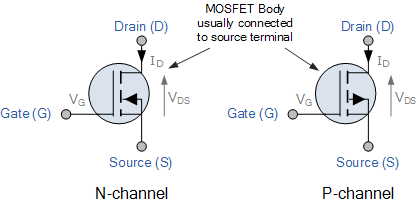
The application of a positive (+ve) gate voltage to a n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.

Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, ID through the channel. In other words, for an n-channel enhancement mode MOSFET: +VGS turns the transistor “ON”, while a zero or -VGS turns the transistor “OFF”. Thus the enhancement-mode MOSFET is equivalent to a “normally-open” switch.

The reverse is true for the p-channel enhancement MOS transistor. When VGS = 0 the device is “OFF” and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it “ON”. Then for an p-channel enhancement mode MOSFET: +VGS turns the transistor “OFF”, while -VGS turns the transistor “ON”.

**Enhancement-mode N-Channel MOSFET and Circuit Symbols**





Enhancement-mode MOSFETs make excellent electronics switches due to their low “ON” resistance and extremely high “OFF” resistance as well as their infinitely high input resistance due to their isolated gate. Enhancement-mode MOSFETs are used in integrated circuits to produce CMOS type *Logic Gates* and power switching circuits in the form of as PMOS (P-channel) and NMOS (N-channel) gates. CMOS actually stands for *Complementary MOS* meaning that the logic device has both PMOS and NMOS within its design.

***BJT as a switch:***

